Claim Amendments

Please amend claims 1, 3, 11-13, 25 and 26 as follows:

Please cancel claims 6, 8-10, 20, and 27-29 as follows:

Please add new claims 32-38 as follows:

1. (currently amended) A method for ~~semiconductor device feature development~~ etching an opening using a bi-layer photoresist to improve an etching resolution and reduce particulate contamination comprising the steps of:

providing an unpatterned non-silicon containing organic resinous layer over a substrate to [from] form a first resist layer;

providing a silicon containing photoresist layer over the first resist layer to form a second resist layer thinner than the first resist layer;

exposing ~~an exposure surface of~~ the second resist layer ~~the second resist layer~~ to form a second resist layer pattern revealing first resist layer portions; ~~and,~~

dry developing said first resist layer portions according to the second resist layer pattern to reveal the substrate ~~in~~ according to a first plasma etching process comprising ~~supplying~~ nitrogen and oxygen to form an etching mask ~~plasma forming gases to form a dry development plasma~~[.];

plasma etching according to a second plasma etching process an opening into the substrate according to the etching mask; and,

carrying out an in-situ ashing process to remove remaining overlying resist layers comprising the first and second resist layers.

2. (cancelled)

3. (currently amended) The method of claim 1, wherein the first resist layer comprises a non-photoactive polymer.

4. (cancelled)

5. (previously presented) The method of claim 1, wherein the activating light source comprises a wavelength selected from the group consisting of about 157 nanometers and about 193 nanometers.

6. (cancelled)

7. (previously presented) The method of claim 6, wherein the first resist layer has a thickness of about 1000 Angstroms to about 5000 Angstroms and the second resist layer has a thickness of about 500 Angstroms to about 3000 Angstroms.

8. - 10. (cancelled)

11. (currently amended) The method of claim 10, wherein the semiconductor feature is selected from the group consisting of a via hole, a trench line, and a contact hole~~, a shallow trench isolation feature, and a polysilicon gate feature~~.

12. (currently amended) The method of claim 1[0], further comprising the step of removing the ~~first~~ second resist layer according to a ~~second~~ first ~~in-situ~~ ashing process ~~following~~ prior to the ~~step of etching~~ second plasma etching process.

13. (currently amended) The method of claim 1[2], wherein the ~~second~~ in-situ ashing process comprises an oxygen containing plasma ~~further comprising at least one of~~ and a component selected from the group consisting of nitrogen and fluorine~~, the oxygen containing plasma~~ to simultaneously clean plasma reactor contact surfaces.

14. - 20. (cancelled)

21. (previously presented) The method of claim 1, wherein the dry development plasma is formed of plasma forming gases consisting essentially of nitrogen and oxygen.

22. (previously presented) The method of claim 1, wherein the dry development plasma is formed of plasma forming gases consisting essentially of nitrogen, oxygen, and argon.

23. (previously presented) The method of claim 1, wherein the first resist layer is selected from the group consisting of an I-line photoresist, an acrylic polymer, and a polyvinyl alcohol polymer.

24. (previously presented) The method of claim 1, wherein the second resist layer comprises a DUV photoresist wherein the silicon comprises silicon incorporated from one of a silylation process and from silicon monomers included in the photoresist.

25. (currently amended) A method for etching a semiconductor device feature using a bi-layer photoresist to improve an opening etching resolution and reduce particulate contamination comprising the steps of:

providing a non-silicon containing ~~organic resinous~~ photoresist layer over a dielectric insulating layer to from a first resist layer;

providing a silicon containing photoresist layer over the first resist layer to form a second resist layer thinner than the first resist layer;

patterning the second resist layer according to a photolithographic exposure process comprising a wavelength ~~less than or equal to about~~ selected from the group consisting of 157 nm and 193 nm;

wet developing the second resist layer to form a patterned second resist layer;

dry etching the first resist layer according to a dry etching chemistry formed by supplying gases consisting essentially of nitrogen, oxygen, and optionally, argon, ~~the first resist layer portions~~ to reveal the dielectric insulating layer to form an etching mask; ~~and,~~

plasma etching in-situ an opening in the dielectric insulating layer [.] according to the etching mask;

carrying out an in-situ oxygen ashing process to remove overlying resist layers comprising at least the first resist layer; and,

carrying out an in-situ plasma cleaning process comprising a component selected from the group consisting of fluorine and nitrogen to clean plasma reactor contact surfaces.

26. (currently amended) The method of claim 25, wherein the second resist layer is removed in-situ according to ~~an~~ a first oxygen ashing process prior to the step of etching.

27. - 29. (cancelled)

30. (previously presented) The method of claim 25, wherein the first resist layer is selected from the group consisting of an I-line photoresist, an acrylic polymer, and a polyvinyl alcohol polymer.

31. (previously presented) The method of claim 25, wherein the second resist layer comprises a DUV photoresist wherein the silicon comprises silicon incorporated from one of a silylation process and from silicon monomers contained within the photoresist.

32. (new) A method for etching a semiconductor device feature using a bi-layer photoresist to improve an opening etching resolution and reduce particulate contamination comprising the steps of:

providing a non-silicon containing photoresist layer over a dielectric insulating layer to from a first resist layer;

providing a silicon containing photoresist layer over the first resist layer to form a second resist layer thinner than the first resist layer;

patterning the second resist layer according to a photolithographic exposure process comprising a wavelength selected from the group consisting of 157 nm and 193 nm;

wet developing the second resist layer to form a patterned second resist layer;

dry etching the first resist layer according to a dry etching chemistry comprising nitrogen, oxygen, and argon, to reveal the dielectric insulating layer to form an etching mask;

carrying out a first in-situ oxygen ashing process to remove the second resist layer;

plasma etching in-situ an opening in the dielectric insulating layer;

carrying out a second in-situ oxygen ashing process to remove the first resist layer;

plasma etching in-situ through a bottom etch stop layer comprising the substrate; and,

carrying out an in-situ plasma cleaning process comprising a component selected from the group consisting of fluorine and nitrogen to clean plasma reactor contact surfaces.

33. (new) The method of claim 32, wherein the first and second in-situ ashing processes comprise adding a component selected from the group consisting of fluorine and nitrogen to simultaneously clean plasma contact surfaces.

34. (new) The method of claim 32, wherein the first resist layer is selected from the group consisting of an I-line photoresist, an acrylic polymer, and a polyvinyl alcohol polymer.

35. (new) The method of claim 1, further comprising the steps of:

etching through a bottom etch stop layer comprising the substrate; and,

carrying out an in-situ plasma cleaning process comprising a component selected from the group consisting of fluorine and nitrogen to clean plasma reactor contact surfaces.

36. (new) The method of claim 1, wherein the first and second plasma etching processes and the ashing process are carried out in a dual source RF power plasma reactor comprising an RF biasing power source.

37. (new) The method of claim 25, wherein the plasma reactor comprises a dual source RF power plasma reactor comprising an RF biasing power source.

38. (new) The method of claim 32, wherein the plasma reactor comprises a dual source RF power plasma reactor comprising an RF biasing power source.